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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,038	07/10/2001	Toshihiro Yamashita	50090-301	6404

7590 04/02/2004

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EXAMINER	
CROWELL, ANNA M	
ART UNIT	**PAPER NUMBER**
1763	

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,038	YAMASHITA ET AL.	
	Examiner	Art Unit	
	Michelle Crowell	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *8-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Akihiro (Japanese Patent Publication 07-240458).

Referring to the Drawing 4, abstract, and paragraphs [0020]-[0026], Akihiro discloses a plasma processing system comprising: a processing chamber 11 into and from which processing gas is inlet and outlet; a pair of electrodes 13, 14 disposed so as to mutually oppose within the processing chamber; a RF feeding apparatus 15 for generating plasma between the pair of electrodes [0026]; a retaining/removal apparatus 12, 17 for retaining a substrate 18 to be processed on and removal from a sample table while one of the pair of electrodes 13 is taken as the sample table; and a detection apparatus 41 for detecting the electrostatic-chucking state of the substrate and for detecting removal state of electrical charges from the substrate, on the basis of variations in impedance arising between the sample table and the substrate. Additionally, the detection apparatus 41 has an impedance detection circuit 46 connected to a power line of the RF feeding apparatus 15 by way of a voltage probe 45. Furthermore, the retaining/removal apparatus includes a DC application apparatus 16 for applying a DC voltage to the sample table.

3. Claims 1, 2, 4, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Deguchi et al. (U.S. 5,665,166).

Referring to the Figure 7, column 4, line 54-column 6, line 48, and column 9, line 26-column 11, line 4 discloses a plasma processing system comprising: a processing chamber 1 into and from which processing gas is inlet 24 and outlet 1a (col. 6, lines 37-48); a pair of electrodes 21, 7 disposed so as to mutually oppose within the processing chamber (col. 5, lines1-7, col. 6, lines 29-36); a RF feeding apparatus 11 for generating plasma between the pair of electrodes (col.5, lines 16-22); a retaining/removal apparatus 8, 32 for retaining a substrate W to be processed on and removal from a sample table while one of the pair of electrodes 7 is taken as the sample table; and a detection apparatus 53 for detecting the electrostatic-chucking state of the substrate and for detecting removal state of electrical charges from the substrate, on the basis of variations in impedance arising between the sample table and the substrate.

With respect to claim 2, the plasma processing system further includes a detection apparatus 53 has an impedance detection circuit 52, 63 connected to a power line of the RF feeding apparatus 11 and the power line of the retaining/removal apparatus 17 by way of a voltage probe 61, the impedance detection circuit detecting plasma impedance stemming from variations in the length of a gap between the sample table and the substrate, the impedance detection circuit detecting an electrostatic chucking failure or the end of removal of electrical charges (col. 10, lines 45-52). Furthermore, the retaining/removal apparatus has an insulating coating 8 provided on the surface of the sample table 7 on which the substrate W is retained.

With respect to claim 4, the plasma processing system includes a RF feeding apparatus which feeds a high-frequency output for producing plasma at 1 KW (col. 7, lines 42-26).

With respect to claim 7, the plasma processing system includes a detection apparatus 53 for detecting a change in plasma impedance on the basis of variations in the length of the gap between the substrate and the sample table 7, the sample table being lowered 33 under lowering pressure of cooling gas inlet 10 from the sample table, the detection apparatus detecting an electrostatic chucking failure (col. 10, lines 21-53, col. 5, lines 8-15, 32-40).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deguchi et al. (U.S. 5,665,166) in view of Collins et al. (U.S. 5,874,361).

The teachings Deguchi et al. are discussed above.

Deguchi et al. fails to teach a DC application apparatus for applying a DC voltage to the

sample table.

Referring to Figure 1 and column 5, lines 41-51, Collins et al. teaches a plasma processing system having a retaining/removal apparatus 122 having an insulating layer 132, a sample table 114, and a DC application apparatus 102 for applying a DC voltage to the sample table 114. By applying a DC voltage to the sample table 114, opposite polarity charges on the wafer and chuck electrode occur which produce an electrostatic attractive force retaining the wafer to the chuck (col. 7, lines 31-43). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide a DC application apparatus for applying a DC voltage to the sample table as taught by Collins et al. as a suitable and equivalent means for retaining a wafer electrostatically.

Deguchi et al. fails to teach a DC voltage within a range of –2.0 KV to 2.0 KV.

Referring to Figures 3-6, column 5, lines 50-56, and column 9, lines 20-column 10, lines 37, Collins et al. teaches a plasma processing system having a retaining/removal apparatus which outputs a chucking voltage for retaining the substrate and outputs a charge-removal voltage for removal of the substrate in the form of a DC voltage within a range of –200 V to 1000V. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the DC voltage within a range of –200 V to 1000 V in order to adequately develop an electrostatic field that electrostatically retains the wafer upon the sample table and releases the wafer from the sample table.

Deguchi et al. fails to teach that a gap between the substrate and the sample table is changed within a range of 0.5 to 15 mm.

Referring to column 7, lines 18-27, Collins et al. teaches a plasma processing system wherein the gap between the substrate 118 and the sample table 122 within a range of 0 to 5 cm for wafer transferring. Additionally, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide a gap between substrate and the sample table within a range of 0 to 5 cm as taught by Collins et al. for wafer transferring.

7. Claim 1 rejected under 35 U.S.C. 103(a) as being unpatentable over Sotozono (Japanese Patent Publication 62-054637) in view of Akihiro (Japanese Patent Publication 07-240458).

Referring to the Drawing 1 and the abstract, Sotozono discloses a plasma processing system comprising: a processing chamber 1 into and from which processing gas is inlet 11, 14 and outlet 13; a pair of electrodes 1, 3; a RF feeding apparatus 10 for generating plasma between the pair of electrodes [0026]; a retaining/removal apparatus 3, 6 for retaining a substrate 5 to be processed on and removal from a sample table while one of the pair of electrodes 3 is taken as the sample table; and a detection apparatus for detecting the electrostatic-chucking state of the substrate and for detecting removal state of electrical charges from the substrate, on the basis of variations in impedance arising between the sample table and the substrate. Additionally, the retaining/removal apparatus has an insulating coating 2 provided on the surface of the sample table 3 on which the substrate is retained. Furthermore, the retaining/removal apparatus includes a DC application apparatus 8 for applying a DC voltage to the sample table. Also, the substrate

is chucked and retained by the sample table by means of the electrostatic force developing between the substrate and the sample table.

Sotozono fails to teach a pair of electrodes disposed within the chamber.

Referring to Drawing 4 and the abstract, Akihiro teaches a plasma processing system wherein the electrodes 13 and 14 are disposed within the chamber 11. Additionally, it is well-known to one of ordinary skill in the art to provide a pair of electrodes within the chamber as a suitable and equivalent means of generating a capacitively coupled plasma. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the electrodes of Sotozono within the chamber as taught by Akihiro since it is a suitable and equivalent means of generating a capacitively coupled plasma.

Response to Arguments

8. Applicant's arguments filed January 14, 2004 have been fully considered but they are not persuasive.

Applicant has argued that Examiner has failed to explain how the voltmeter of Akihiro identically describes the claimed impedance detection circuit since voltage and impedance are two different electrical characteristics that are not considered comparable by one having ordinary skill in the art. However, it is well known to one having ordinary skill in the art that impedance equals voltage divided by current (impedance=V/I) (see Burns article-Impedance Measurements). Therefore, when voltage is measured, the impedance can be determined. Impedance and voltage have a direct relationship, so when current is constant and voltage increases, hence the impedance increases. Furthermore, it should be noted that only claim 1 was

rejected under 35 U.S.C. 102 by Akihioro, and since claim 1 fails to require an impedance detection circuit, Akihiro still satisfies the claimed requirement.

Applicant has argued that the Examiner has failed to explain how current monitor and a DC voltage monitor in Deguchi et al. correspond to the claimed impedance detection circuit when current/voltage are not comparable to impedance. However, it is well known to one having ordinary skill in the art that impedance equals voltage divided by current (Z=V/I). Therefore, when voltage and/or current is measured, the impedance can be determined. Furthermore, Deguchi et al. clearly states that the plasma impedance(discharge) and sample location is detected through the use voltage and current monitors (col. 10, lines 45-52).

Applicant has argued that Examiner has failed to indicate where the claimed detection apparatus can be found in Sotozono. However, the purpose portion of the abstract clearly states that the invention of Sotozono includes a device for detecting voltage and detecting a setting state of the chucked work from the voltage value. As previously discussed, it is well known to one having ordinary skill in the art that impedance equals voltage divided by current (impedance=V/I). Therefore, when voltage is measured, the impedance can be determined. Impedance and voltage have a direct relationship, so when current is constant and voltage increases, hence the impedance increases. Furthermore, it should be noted that only claim 1 was rejected under 35 U.S.C. 103 by Sotozono in view of Akihiro, and since claim 1 fails to require an impedance detection circuit, Sotozono in view of Akihiro still satisfies the claimed requirement.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Crowell whose telephone number is (571) 272-1432. The examiner can normally be reached on M-F (8:00 - 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Mills can be reached on (571) 272-1439. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AMC
03-26-04

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